MULTIPLE DATA STATE MEMORY CELL

TECHNICAL FIELD

The invention relates to random access memories ("RAMs"), and more particularly to memory cells of a RAM capable of storing data in multiple data states.

BACKGROUND OF THE INVENTION

Random access memory devices are an integral part of any computing environment. Without these memory devices, processing data in a computing device would be nearly impossible. Consequently, there has been a great amount of research and development directed to the area of random access computer memory. The research and development has been directed to different areas related to computer memory, for example, in increasing the speed at which data stored by the memory devices can be accessed, in designing memories with lower power consumption, and in engineering memory devices having greater data retention times. Additionally, one particular area to which a great amount of effort has been spent is in the areas of increasing memory density and data capacity.

One conventional approach to increasing memory density has been to decrease the size of memory devices, and more particularly, decrease the size of memory cells. As a result, the size of memory cells have been reduced dramatically in the recent past. However, the size of memory cells have diminished to the point where the current state of processing technology is being constantly challenged when manufacturing memory devices with these feature sizes. Another approach to the memory density and data capacity issue has been experiment with memory devices that are capable of storing data in more states than conventional binary memory. That is, conventional memory stores data in a binary format, where data is stored as either one of two different data states. With multiple data state memory, data can be stored as one of many different states, where the number of different states is greater than two. As a result, with multiple data state memory,

generally less memory cells need to be used to store data. For example, a memory cell having four different data states can be substituted for two conventional memory cells having only two different data states. Consequently, only half as many memory cells would be needed to store the same quantity of data. Conversely, twice as much data can be stored in the same area if the multiple data state memory is the same size as conventional memory cells.

An example of the type of work that has been done in the area of multiple data state memory is provided in several U.S. Patents to Ovshinsky *et al.* For example, in U.S. Patent No. 5,296,716 to Ovshinsky *et al.*, the use of electrically writeable and erasable phase change materials for electronic memory applications is described. Additionally, in U.S. Patent No. 5,912,839 to Ovshinsky et al., a method of programming Ovonic memory multistate-digital multibit memory elements and the use in data storage is described. As described therein, a memory element including the phase change material, that is, materials which can be electrically switched between generally amorphous and generally crystalline, can be programmed by using a number of current pulses. In determining the data state of the memory element, the number of pulses can be discerned by counting the number of pulses required to return the resistance level of the memory element to a first state. The number of pulses represents the data state of the data stored by the memory element. As further described in the aforementioned patent, the process of reading the present state of the memory element is destructive, and consequently, requires that the data is reprogrammed following a read.

Another approach that has been taken in the design of multiple data state memory is described in U.S. Patents to Kozicki et al. As described therein, a programmable metallization cell (PMC) formed from a fast ion conductor, such as a chalcogenide material that include compounds containing sulfur, selenium and tellurium, positioned between two electrodes. The formation of a non-volatile metal dendrite can be induced by application of a voltage difference between the two electrodes. The mass of the non-volatile dendrite changes the resistance of the PMC, which can be used as a means to

store data in various states. Further described in the aforementioned patents are various structural embodiments of a PMC in different applications.

Although there has been development in the area of multiple data state and variable resistance memories, it will be appreciated that new and alternative approaches to this area is still possible. For example, further development in the area of multiple data state memory cells having true quantization of data states. Therefore, there is a need for alternative approaches to storing data in multiple data states.

SUMMARY OF THE INVENTION

The present invention is directed to a multiple data state memory cell. The memory cell includes a first electrode layer formed from a first conductive material, a second electrode layer formed from a second conductive material, and a first layer of a metal-doped chalcogenide material disposed between the first and second electrode layers, the first layer providing a medium in which a conductive growth can be formed to electrically couple together the first and second electrode layers. The memory cell further includes a third electrode layer formed from a third conductive material, and a second layer of a metal-doped chalcogenide material disposed between the second and third electrode layers, the second layer providing a medium in which a conductive growth can be formed to electrically couple together the second and third electrode layers.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional view of an embodiment of the invention.

Figures 2a-c are cross-sectional views of the embodiment of Figure 1 illustrating the operation thereof.

Figure 3 is a cross-sectional view of another embodiment of the invention.

Figure 4 is a block diagram of a typical memory device that includes one or more memory arrays of the present embodiment.

As is conventional in the field of integrated circuit representation, the lateral sizes and thicknesses of the various layers are not drawn to scale and may have been enlarged or reduced to improve drawing legibility.

DETAILED DESCRIPTION OF THE INVENTION

Embodiments of the present invention provide a multiple state memory cell. Certain details are set forth below to provide a sufficient understanding of the invention. However, it will be clear to one skilled in the art that the invention may be practiced without these particular details. In other instances, well-known fabrication techniques processing methods, circuits, control signals, and timing protocols have not been shown in detail in order to avoid unnecessarily obscuring the invention.

Illustrated in Figure 1 is a cross-sectional view of a portion of a multiple-state memory cell 200 according to an embodiment of the present invention. A metal electrode layer 202 is formed to provide a cathode layer to which a voltage is applied. It will be appreciated that the metal layer 200 may be formed on a substrate, or on a layer of material which will support the multiple-state memory cell 200. Formed on the metal layer 200 is a metal-doped chalcogenide layer 204 through which, as will be explained in more detail below, a conductive link to floating electrode layer 206 is formed under the application of a voltage. Chalcogenide materials, as referred to herein, include those compounds of sulfur, selenium, and tellurium. The metal material doping the chalcogenide are generally Group I or Group II metals, such as silver, copper, zinc, and combinations thereof. The floating electrode layer 206 is typically formed from a metal material, such as silver.

Formed on the floating electrode layer 206 is a another metal-doped chalcogenide layer 208. The composition of the material for layer 208 may be, but does not necessarily need to be, the same as the layer 204. As illustrated in Figure 2, the thickness t_2 of the layer 208 is greater than the thickness t_1 of the layer 204. However, in other embodiments of the present invention, the thicknesses t_2 and t_1 may be nearly or

approximately the same, or the thickness t_2 may be less than t_1. As will be explained in more detail below, the composition of the respective metal-doped chalcogenide layers 206 and 208 may need to be modified in order to accommodate layers 206 and 208 having various thicknesses. Formed on the metal-doped chalcogenide layer 208 is another metal electrode layer 210, which represents an anode of the multiple-state memory cell 200. The metal electrode layer 210 and the floating electrode layer 206 are typically formed from the same material. As illustrated in Figure 1, the cathode is formed below the anode, however, it will be appreciated that the arrangement of the two layers may be reversed as well without departing from the scope of the present invention. Moreover, the vertical orientation illustrated in Figure 1 can be changed such that the various layers are formed in a horizontal orientation between a cathode and an anode that are laterally spaced apart from one another.

It will be appreciated that many materials known by those of ordinary skill in the art may be used for the metal-doped chalcogenide layers. For example, compositions of germanium selenide, Ge_xSe_y, can be used. Exemplary ratios are in the range from $Ge_{20}Se_{80}$ to GeSe. Compositions of arsenic sulfide, germanium telluride, and germanium sulfide can also be used for the metal-doped chalcogenide layers. Similarly, materials that can be used for the electrode layers are also known, such as silver, compositions of silver selenide, copper, germanium selenide, and the like. It will be appreciated that later developed materials that display the same characteristics as known materials can also be used for the metal-doped chalcogenide and electrode layers without deviating from the scope of the present invention.

In operation, the multiple-state memory cell 200 illustrated in Figure 1 is capable of storing multiple states by altering or programming the total resistance between the anode and the cathode in a relatively digital fashion. The resistance of the memory cell 200 can then measured or compared to determine the value of the data stored by the memory cell 200. As a result of the relatively discrete manner in which the resistance can be changed, multiple states can be stored by the memory cell 200.

The alteration of the resistance is accomplished by the formation of a conductive growth from the metal electrode layer 202 (*i.e.*, the cathode) through the layer 204 to electrically contact the floating electrode layer 206, and the formation of a conductive growth from the floating electrode layer 206 through the layer 208 to electrically contact the metal electrode layer 210 (*i.e.*, the anode). The formation of the conductive growth is induced by creating a voltage difference between the cathode and the anode, such as by applying a voltage to the anode and grounding the cathode.

Each time a conductive growth creates a short circuit, the resistance between the anode and the cathode changes relatively significantly. Initially, as shown in Figure 2a, where no conductive growth has been formed, the resistance between the anode and the cathode R_{cell} is equal to approximately $R_1 + R_2$, where R_1 is the resistance of the layer 204 and R_2 is the resistance of the layer 208. However, under the influence of an applied bias across the metal-doped chalcogenide layers 202, 210, conductive growths 304 and 308 begin to form through the layers 204 and 208, respectively. When the conductive growth 308 extends through the layer 208 and creates a short circuit between the the floating electrode layer 206 and the anode, which is represented by the layer 210, as shown in Figure 2b, the resistance R_{cell} between the anode and the cathode changes to a value less than R_1 but greater than a short circuit. The resistance R_{cell} at this point is reproducible, and consequently, can be used to represent a data state. The resistance R_{cell} changes again, as shown in Figure 2c, to a relatively low resistance when a conductive growth 304 extends through the layer 204 and creates a short circuit between the cathode, which is represented by the layer 202, and the floating electrode layer 206.

Each of the different resistance states of R_{cell} provided by the memory cell 200 represents a different data or logic state. That is, a first data state is represented by R_{cell} being approximately equal to the total resistance (R1+R2), a second data state is represented by R_{cell} being a value between R_1 and low resistance, which occurs when the floating electrode layer 206 is short circuited to the metal electrode layer 210 by the conductive growth 308, and a third data state is represented by a low resistance after the

metal electrode layer 202 is short circuited to the floating electrode layer 206 by the conductive growth 304. A reading circuit coupled to the memory cell 200 measures the resistance of the memory cell 200 in order to determine the data stored by the cell.

The growth of the conductive growths 304 and 308 is dependent on the orientation of the electrical field applied to the memory cell 200. That is, as discussed so far, a voltage applied to the metal electrode layer 210 (*i.e.*, the anode) is positive relative to the voltage applied to the metal electrode layer 202 (*i.e.*, the cathode), thus, the direction of growth is from the metal electrode layer 202 to the floating electrode layer 206. Similarly, a conductive growth will be formed extending from the floating electrode layer 206 to the metal electrode layer 210. However, it will be appreciated that application of the voltage in an opposite polarity will reduce whatever conductive growth has been previously formed. Consequently, the memory cell 200 can be programmed to store a different data state by changing the polarity of the applied voltage to the memory cell 200 during a read or write operation to change the resistance of the memory cell 200.

It will be further appreciated that reading and writing circuitry for use with embodiments of the present invention is well known to those of ordinary skill in the art, and may be implemented using conventional circuitry and design. It will be further appreciated that the description provided herein is sufficient to enable one of ordinary skill in the art to practice the invention.

As illustrated in Figure 2b, application of a voltage to the anode induces the formation of not only conductive growth 304, but conductive growth 308 as well. However, because the thickness of the layer 208 is greater than the thickness of the layer 204, for a given applied voltage across the multiple state memory cell 200 the voltage across the layer 208 is greater than the voltage across the layer 204. Consequently, the floating electrode 206 is short circuited to the anode before the cathode is short circuited to the floating electrode 206. With continued application of a voltage to the anode, the conductive growth 304 eventually creates a short circuit between the cathode and the floating electrode 206, thus reducing the resistance between the anode and the cathode to a

low resistance. Moreover, it will be appreciated that the resistance R_{cell} across the anode and cathode is between R_1 and a short circuit after the conductive growth 308 short circuits the floating electrode 206 to the anode 210 because the resistance of the layer 204 is actually reduced as the conductive growth 304 grows toward the floating electrode 206. However, the resistance R_{cell} at this point is nevertheless reproducible and different enough from the short circuited state that conventional reading circuits for multiple-state memory cells can consistently recognize the data state.

It will be further appreciated that the range of resistances, or the transition from one resistance relative to one another can be adjusted by altering the thickness of the layers 204 and/or 208. Additionally, as previously mentioned, the composition of the metal-doped chalcogenide material of the layers 204 and 208 can be adjusted as well to adjust the points of transition in the resistance.

Illustrated in Figure 3 is a portion of a memory cell 400 according to another embodiment of the present invention. The memory cell 400 includes layers that are similar to those of the memory cell 200 (Figure 1). However, memory cell 400 further includes a second floating electrode 420 and a third metal-doped chalcogenide layer 424 in addition to the layers described with respect to the memory cell 200. The addition of the second floating electrode 420 and the third metal-doped chalcogenide layer 424 enables the memory cell 400 to have an additional memory state in which to store data. That is, whereas the memory cell 200 provides three different states or resistances R_{cell}: $(R_2 + R_1)$, between R_1 and low resistance, and low resistance, the memory cell 400 provides four different states or resistances for R_{cell}: $(R_3 + R_2 + R_1)$, between $(R_2 + R_1)$ and R_1, between R_1 and low resistance, and low resistance. As previously discussed, each different resistance level can be used to represent a different state of data.

As illustrated by the previous discussion, it will be appreciated that including additional layers formed from a metal-doped chalcogenide material and a floating electrode can be used to create memory cells having even more states than that provided by the memory cell 400.

A memory device 500 that includes a memory array 502 having memory cells according to an embodiment of the invention is shown in Figure 4. The memory device 500 includes a command decoder 506 that receives memory command through a command bus 508 and generates corresponding control signals. A row or column address is applied to the memory device 500 through an address bus 520 and is decoded by a row address decoder 524 or a column address decoder 528, respectively. Memory array read/write circuitry 530 are coupled to the array 502 to provide read data to a data output buffer 534 via a input-output data bus 540. Write data are applied to the memory array through a data input buffer 544 and the memory array read/write circuitry 530.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.